IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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marsha
5/15/03

In re application of:

H. Ikeda et al.

Application No.: 09/917,913

Filed: July 31, 2001

Group Art Unit: 2818

Examiner: C. Yoha

Docket No.: 100353-00065

For: SEMICONDUCTOR MEMORY DEVICE HAVING AN SRAM AND A DRAM ON A SINGLE CHIP

RESPONSE UNDER 37 C.F.R. § 1.121

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 12, 2003

Sir:

In reply to the Office Action mailed February 10, 2003, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claim 9.

Please amend the claims as follows. A copy of the marked-up original claims is attached to this Response showing the changes, as required by amended 37 C.F.R. §1.121.

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8. (Amended) A semiconductor memory device comprising:

an SRAM memory block provided on a chip, the SRAM memory block including a first power pad and an SRAM cell array connected to the first power pad;

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a DRAM memory block provided on the chip, the DRAM memory block including a second power pad and a DRAM cell array connected to the second power pad; and

a control unit controlling ON/OFF of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is